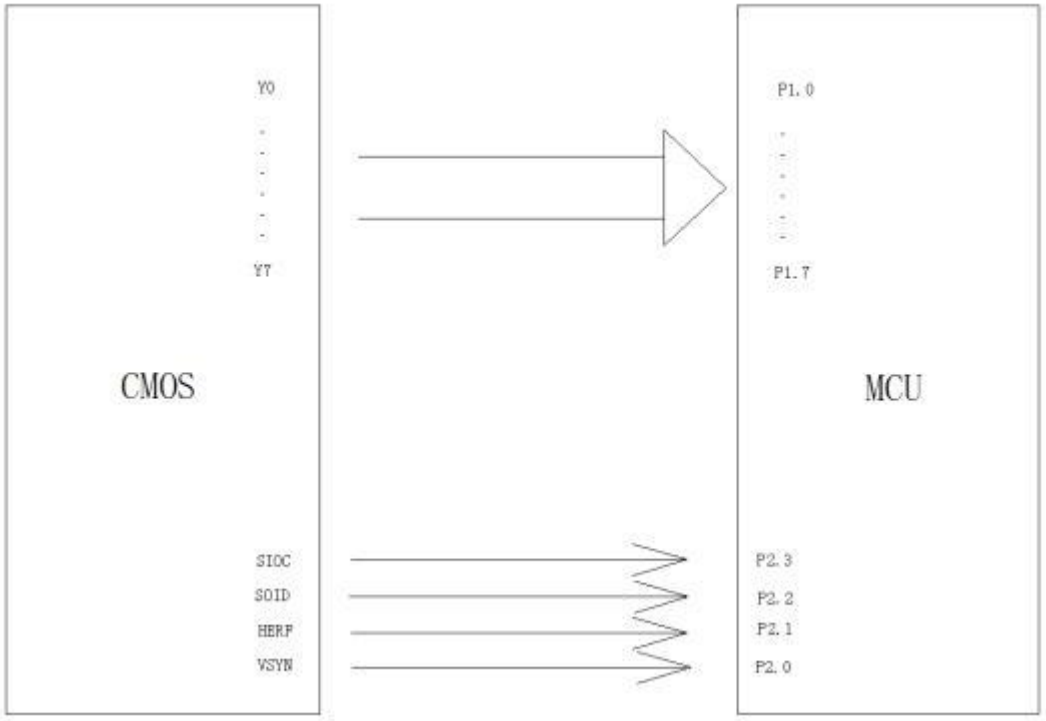
FIFO

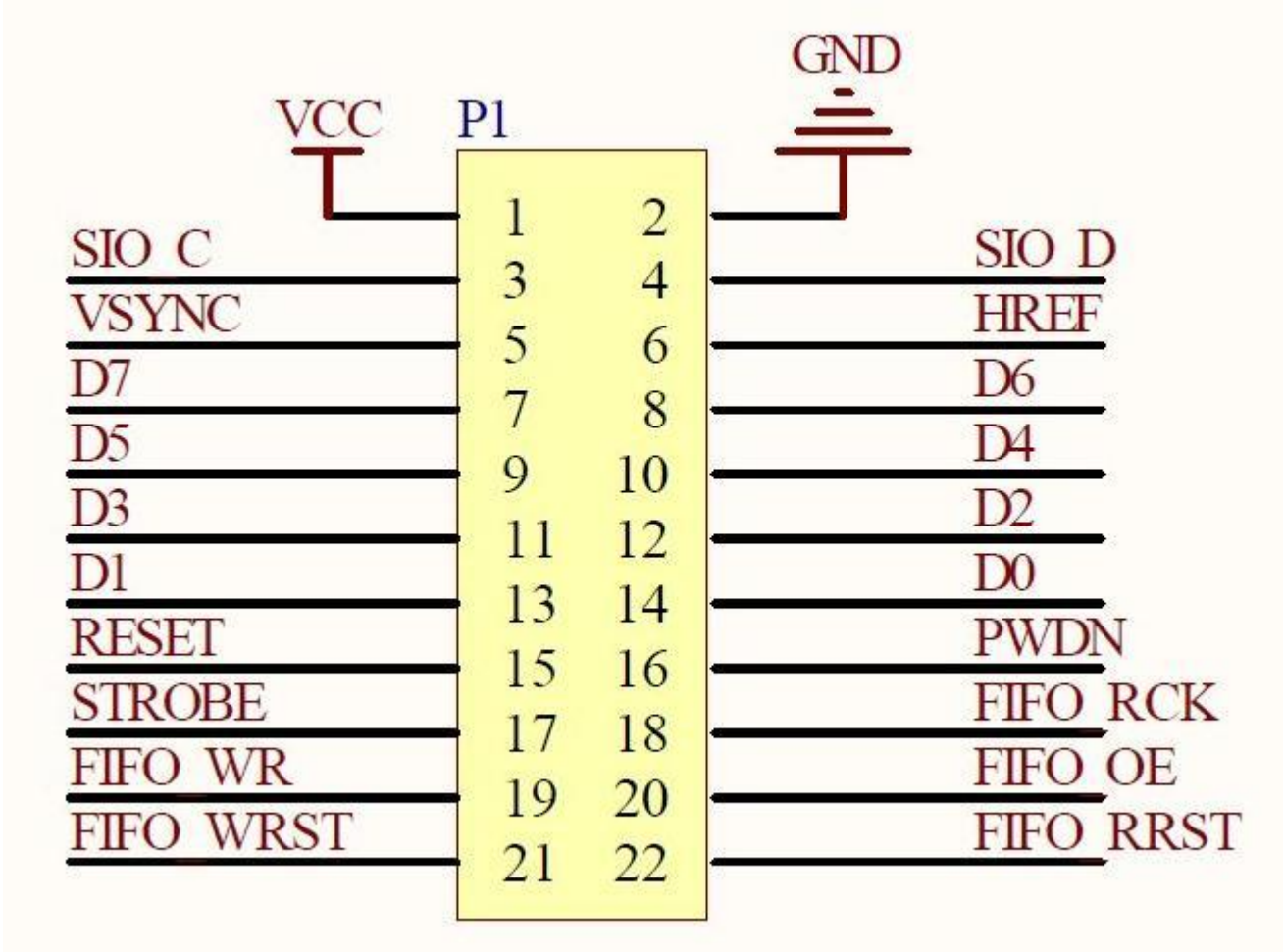
Basic Principle

OV7670 FIFO camera, image sensor and image buffer pieces AL422B combine to solve the problem of low-end microcontroller image acquisition speed bottleneck. Basic principle:



User according to the figure above simply the fifo read data timing control pin, data can be read directly by the MCU IO port data into memory or sent to the screen memory display can be operated by low-speed MCU control, and simple processing of the data, such as black and white identification.

The OV7670 with FIFO module, image acquisition and control with buffer storage space a module is able to slow the MCU. This module adds a FIFO (first-in, first-out) memory chips, the same 30w-pixel CMOS image photosensitive chip, 3.6mm focal length of the lens and the lens mount, onboard various power CMOS chip (power requirements are detailed in chip data file), the board at the same time leads to the control pins and data pins, easy to operate and use.


GND
VCC
P1
1
2
SIO_C
3
4
SIO_D
VSYNC
5
6
HREF
D7
7
8
D6
D5
9
10
D4
D3
11
12
D2
D1
13
14
D0
RESET
15
16
PWDN
STROBE
17
18
FIFO_RCK
FIFO_WR
19
20
FIFO_OE
FIFO_WRST
21
22
FIFO_RRST

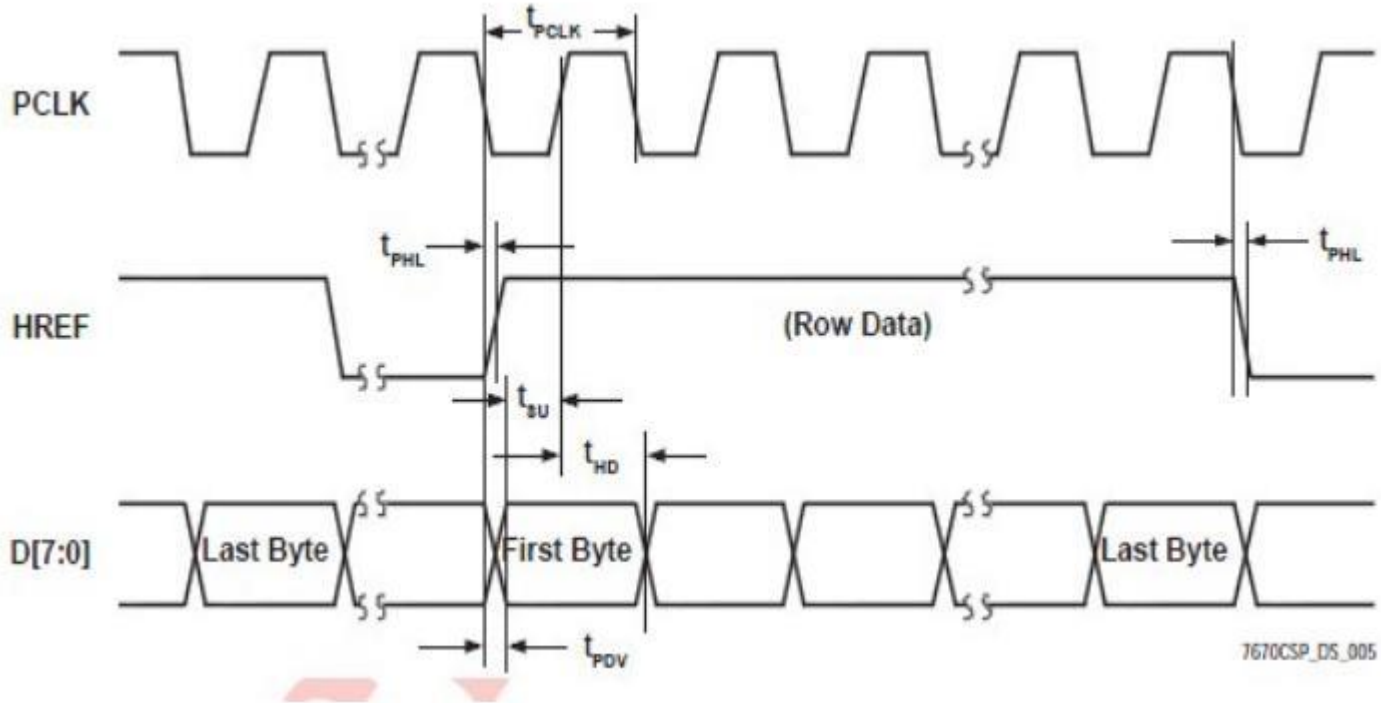
As control sensor pin defined as follows:

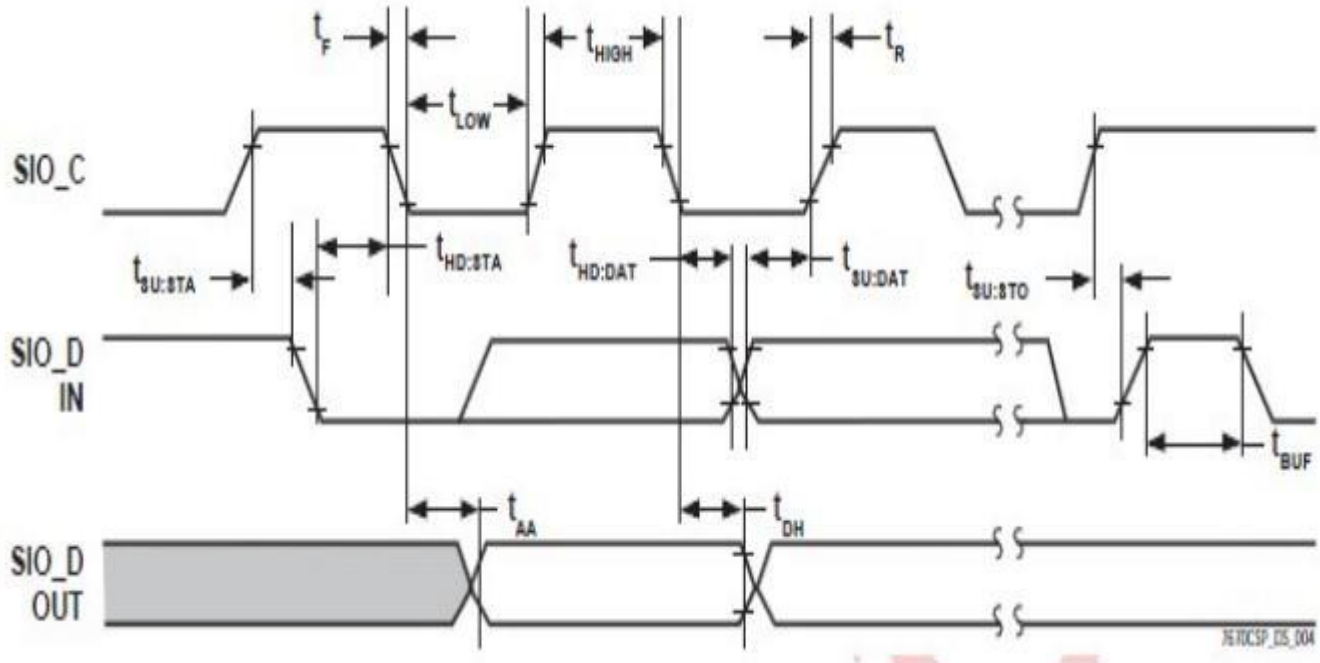
- 3V3 ----- input supply voltage (recommended 3.3,5 V can also be, but is not recommended)
- The GDN ----- ground point
- SIO_C --- SCCB interface control clock (Note: some of the low-level microcontroller needs pull-up control, and the I2C interface similar)
- SIO_D --- SCCB interface serial data input (output) end (Note: some of the low-level microcontroller needs pull-up control, and the I2C interface similar)
- VSYNC --- frame synchronizing signal (output signal)
- HREF ---- line synchronizing signal (the output signal, can generally not applicable to use of special cases)
- D0-D7 --- data port (output signal)
- RESTE --- reset port (normal use pulled)
- PWDN ---- power selection mode (normal use pull down)
- The STROBE-photographed flash control port (normal use may not be required)
- FIFO_RCK --- FIFO memory read clock control terminal
- FIFO_WR_CTR ---- FIFO write control terminal (1 allows the CMOS is written to the FIFO, to prohibit 0)
- FIFO_OE ---- FIFO off control
- FIFO_WRST-FIFO write pointer reset terminal
- FIFO_RRST-FIFO read pointer reset terminal

Sequence

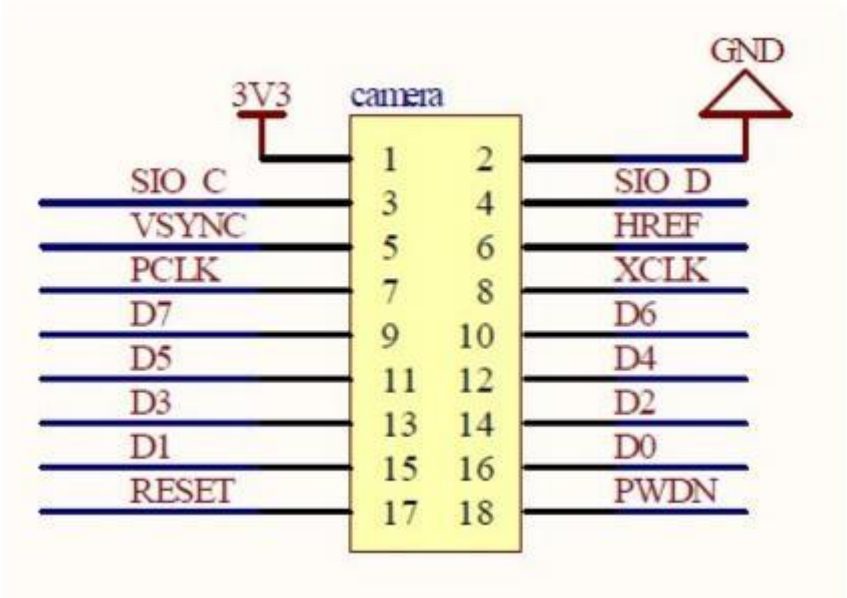
Using the FIFO as data buffering, data acquisition is greatly simple, users only need to be concerned about is how to read, do not need to worry about how specific data is collected, it can be reduced or even do not care about the CMOS control and timing relationships,image acquisition.

Control sequence is as follows:





Without FIFO



Pin Definition

- 3V3 ----- input supply voltage (recommended 3.3,5 V can also be, but is not recommended)
- The GDN ----- ground
- SIO_C --- SCCB interface control clock (Note: some of the low-level microcontroller needs pull-up control, and the I2C interface similar)
- SIO_D --- SCCB interface serial data input (output) end (Note: some of the low-level microcontroller needs pull-up control, and the I2C interface similar)
- VSYNC --- frame synchronizing signal (output signal)
- HREF ---- line synchronizing signal (output signal)
- The PCLK ---- pixel clock (output signals)
- D0-D7 --- data port (output signal)
- RESTE --- reset port (normal use pulled)
- PWDN ---- power selection mode (normal use pull down)